18.1 A 25Gb/s CDR in 90nm CMOS for High-Density Interconnects

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High-density electrical and optical backplane systems typically employ pre-defined reference frequencies that are usually multiplied from a quartz crystal oscillator with a frequency tolerance ranging from ±10 to ±100ppm. A phase detector (PD) for random data streams detects a phase error and has the ability to adjust small frequency errors. As a result, a phase-detecting CDR topology is sufficient for source-synchronous systems.

The block diagram of the implemented CDR is shown in Fig. 18.1.1. A static frequency divider divides the external reference clock (f_{ref}) by 2. The outputs are 2 differential clocks shifted by 90°, commonly referred to as I and Q. Consequently, clock phases at 0°, 90°, 180°, and 270° at half the reference clock frequency (half-rate) are generated. In each phase quadrant, a phase interpolator (PI) (Fig. 18.1.2) interpolates the clock phases by a factor of 8. This results in a total of 32 phase steps in the 360° (2π) phase circle of the half-rate clock and in 16 phase steps with respect to the full rate. The phase-adjusted clock is buffered at the output of the PI to drive the large capacitive load of the linear half-rate phase-detector (LHRPD) and the D-flip-flops (DFF) of the data synchronization pipeline (Fig. 18.1.3). The half-rate clock is divided by 32 to clock the slow digital loop filter and control logic. The LHRDP measures the phase error (ERR) between incoming random data and the clock with respect to a reference pulse (REF) and feeds it to an analog filter (Fig. 18.1.4). In the analog filter, twice the ERR is subtracted from REF to generate a phase error with respect to the center of the data pulse (DIF) and then integrated over time (DIF_{avg}). This integrated analog signal is limited, digitally sampled, and fed to the digital 7 to 10b loop filter counter as an up-or-down-count signal (DIR). The 2b LBWS switch can select the counter size and thus the CDR loop dynamics. The 5 MSBs of the counter adjust the clock phase in the PI after passing a thermometer encoder.

A systematic analysis of a first-order bang-bang (BB) PLL is performed in [1], where its loop behavior is described using ΔΣ conversion theory in the phase domain. The lock range condition yields: $-f_{bb}<\Delta f<f_{bb}$, where $f_{bb}=f_{ref}/2^N$ denotes the maximum frequency deviation between f_{ref} and the nominal data rate frequency f_{nom}, and $\Delta f = f_{nom}-f_{ref}$. The frequency divider and the selectable digital loop counter size determine the parameter N={13,14,15,16} for LBWS=["00","01","10","11"], respectively. For LBWS="00", f_{bb}/f_{ref} yields 122ppm. If Δf=0, the slew-rate limited phase modulation amplitude is $A_{UIpp}=DTD\times f_{bb}/f_{mod}$, where f_{mod} stands for the phase modulation frequency, and DTD represents the data transition density and yields a value of $\sim^1/_2$ for PRBS. These results indicate that the CDR loop dynamics are controlled by f_{bb}.

The implemented CDR topology offers 4 advantages: First, the digital loop filter eliminates the need for large analog loop-filter capacitors and enables an accurate control of the loop dynamics. Second, a digital controlled phase rotator circumvents the use of an oscillator or delay line for each CDR in a high-density link. Third, for the chosen CDR scheme, a half-rate PD is required, which has the advantage of higher speed, compared to a full-rate PD as the latches (TFF) run at half the speed. Fourth, the analog filter and limiter consume less power than a digital implementation.

The LHRPD in [2] consists of 4 TFF and 2 XOR gates. For comparison, the Alexander PD [3] is a non-linear type and when implemented as a half-rate PD, requires 16 TFFs. The capacitive loads of the XOR gates in the data pipeline can result in a speed limitation of the entire CDR. Short ERR signal pulses are low-pass-filtered, leading to inaccurate PD error detection, and data errors due to metastability in the DFF. To minimize the capacitive loads at the output of the TFFs, the topology in [2] is parallelized, yielding the proposed LHRPD in Fig. 18.1.3. It works the same as the conventional circuit, but the speed is increased by a factor of ~2. The cost of this speed optimization is an increase of the number of CML TFFs from 4 to 10, which is still less than what the half-rate Alexander PD requires. The core LHRPD is formed by TFF[1:2], DFF[1:4] and XOR gates. DFF[5:8] are added to further synchronize the data and minimize bit errors due to FF metastability. At the half-rate data and clock outputs, 50Ω CML buffers (BUF) are included to drive test and measurement equipment.

The circuit schematic of the analog filter is shown in Fig. 18.1.4. The operation of DIF=2×ERR-REF is performed by adding the inverse differential currents of the REF and the ERR signals, and by device scaling. Thus, transistors $M_{4A,B}$ have twice the width of $M_{3A,B}$. The dummy load transistors $M_{2A,B}$ balance the capacitive loads of the REF and ERR signals. A source-degeneration topology of the current-summing differential pairs is chosen for low voltage gain to avoid signal saturation and to improve linearity of the analog operation. Transistors $M_{1A,B}$ allow the sampling point to be changed in time by tuning the RATIO signal at the current source and to compensate for PD inaccuracy at high speed. An analog lock detector determines the locked condition (LOCK="1") if the variation of DIF_{avg} drops below a selectable reference value. The implemented CDR operates from 8 to 28Gb/s and yields a BER of $<10^{-12}$ at the output of the half-rate data channels and combined at full-rate for PRBS 2^7-1. The differential input data signal amplitude is $620mV_{pp}$. Calculated and measured f_{bb} values are consistent for all selectable values of N. The CDR yields a random, deterministic, and total timing jitter at a BER=10^{-12} of 0.96ps, 4ps, and 17.3ps, respectively, of the half-rate data outputs (Fig. 18.1.5) and a phase noise of -108.8dBc/Hz of the recovered clock at a frequency offset of 10MHz from the carrier for LBWS="11". The jitter tolerance for all selectable values of LBWS is $>0.35UI_{pp}$ for sinusoidal jitter frequencies ≤100MHz (Fig. 18.1.6). The total power consumption of the implemented circuits amounts to 172mW from a 1.1V supply, where the output buffers consume 22mW, the input reference clock buffer 28mW, the input 50Ω termination 24mW and the core CDR circuit 98mW. This results in a total power consumption per data rate for the core CDR of 3.9mW/(Gb/s). The core circuit occupies a chip area of 0.32×0.22mm², implemented in a 90nm CMOS 8M process. A chip micrograph of the designed CDR with the main circuit blocks labeled is shown in Fig. 18.1.7.

The low-power CDR topology is suited for future high-density chip-to-chip interconnects with aggregate throughputs of multiple Tb/s.

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References:
[1] R. C. Walker, "Designing Bang-Bang PLLs for Clock and Data Recovery in Serial Data Transmission Systems," in: "Phase-Locking in High-Performance Systems - From Devices to Architectures" ed: by Behzad Razavi, *IEEE Press*, 2003, pp. 34-45.
[2] J. Savoj, and B. Razavi, "A 10-Gb/s CMOS Clock and Data Recovery Circuit With a Half-Rate Binary Phase/Frequency Detector," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 13-21, Jan., 2003.
[3] J. D. H. Alexander, "Clock Recovery from Random Binary Data," *Electronic Letters,* vol. 11,pp. 541-542, Oct., 1975.

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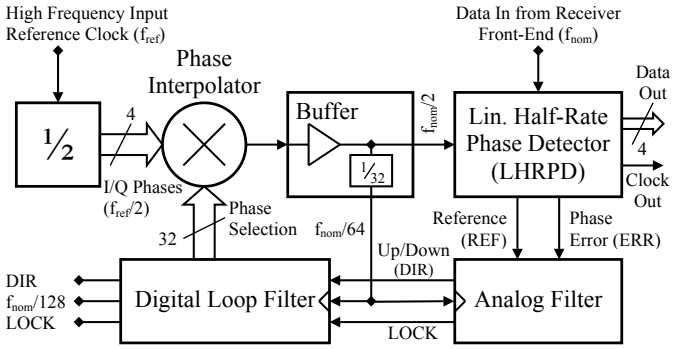

Figure 18.1.1: Block diagram of the designed clock-and-data recovery circuit.

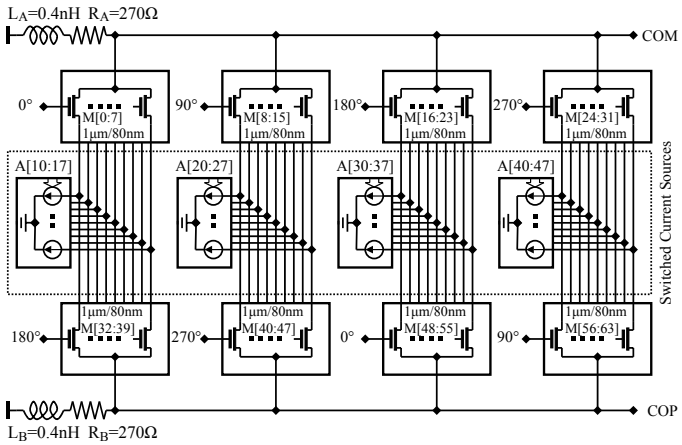

Figure 18.1.2: Block diagram of the differential phase interpolator.

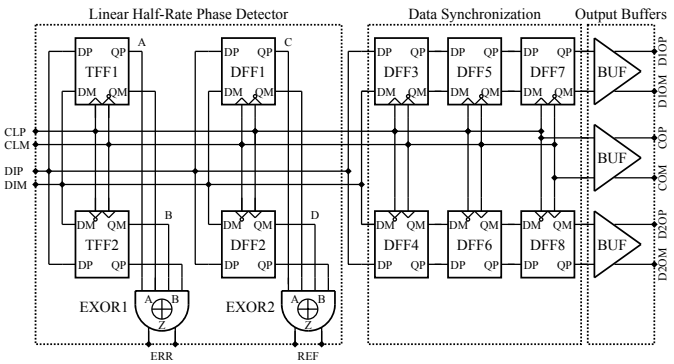

Figure 18.1.3: Block diagram of the speed-improved half-rate linear phase detector.

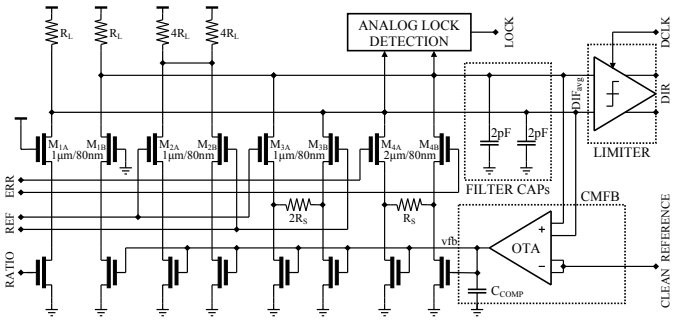

Figure 18.1.4: Schematic of the analog filter and limiter.

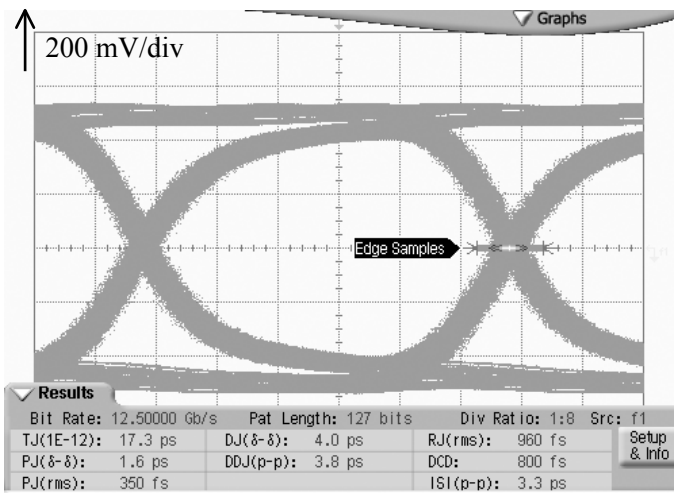

Figure 18.1.5: Eye-diagram and jitter measurement of one half-rate differential data output of the CDR.

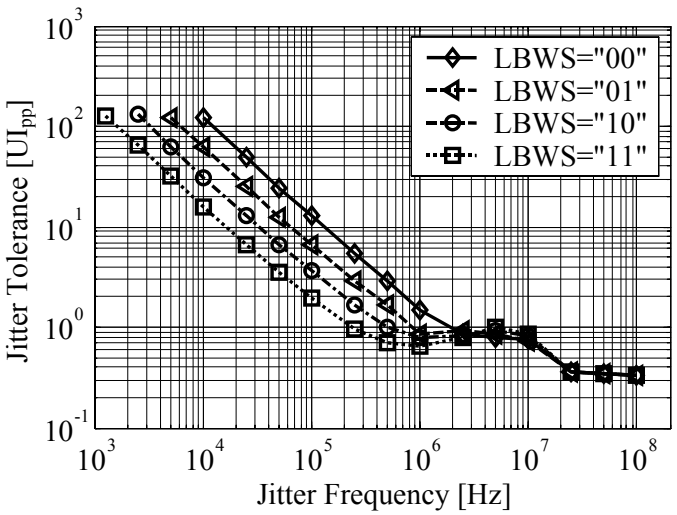

Figure 18.1.6: Measured jitter tolerance curves for different loop bandwidths.

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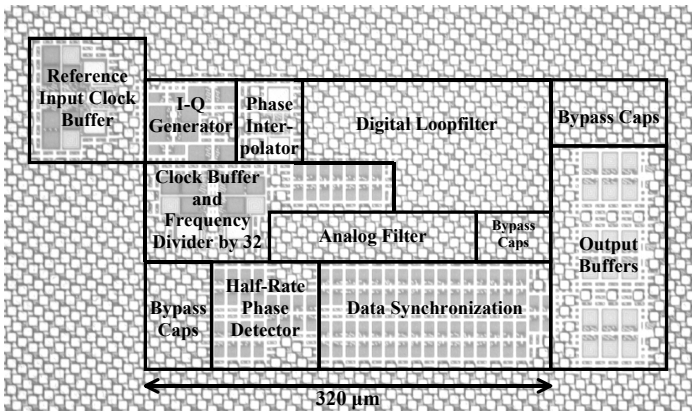

Figure 18.1.7: Chip micrograph of the designed CDR featuring a die size of 320µm×220µm (0.07mm²) excluding the input and output buffers.

